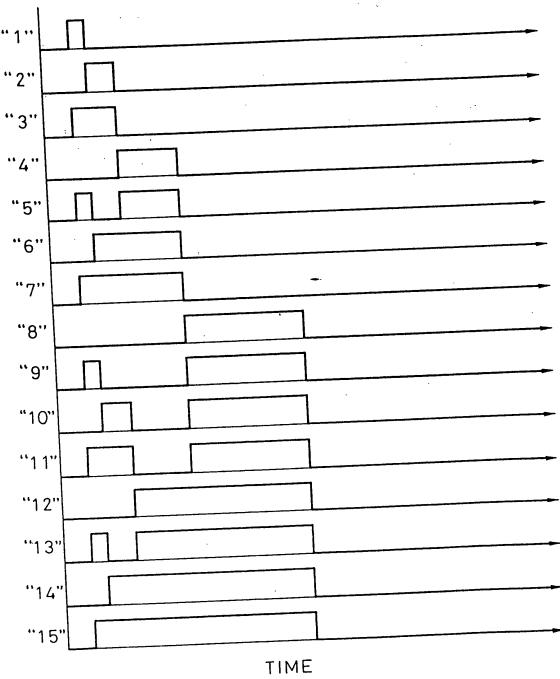
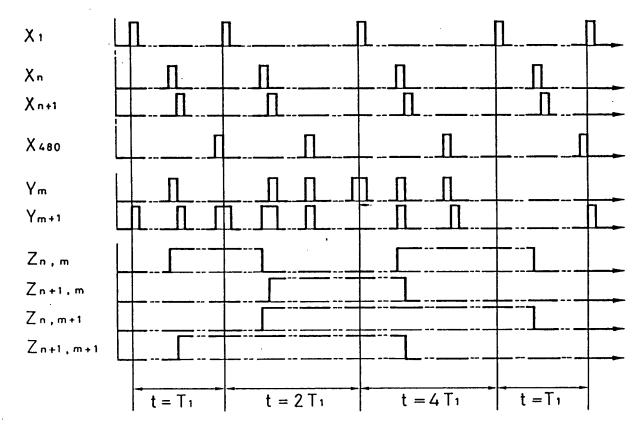
FIG.1



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FIG. 2



 $Z_{n,m}$: $T_1 + 4T_1 = 5T_1$ —— "5" $Z_{n+1,m}$: $2T_1$ —— "2" $Z_{n,m+1}$: $2T_1 + 4T_1 = 6T_1$ —— "6" $Z_{n+1,m+1}$: $T_1 + 2T_1 = 3T_1$ —— "3"

.

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FIG. 3

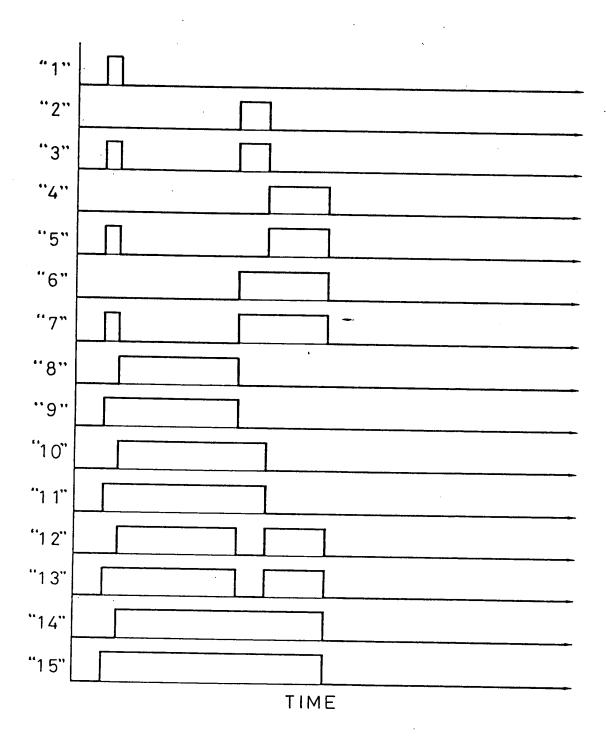
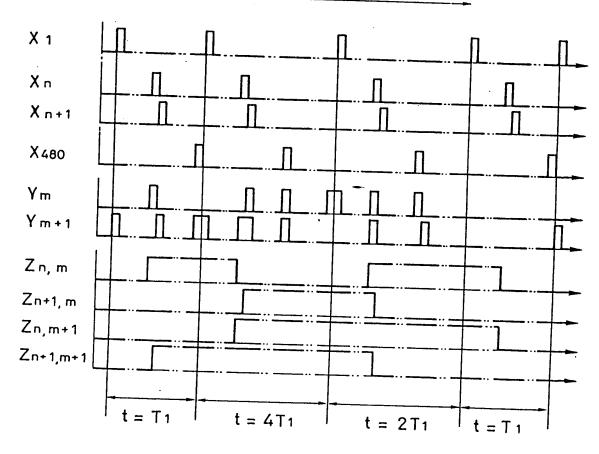


FIG. 4

1 SCREEN



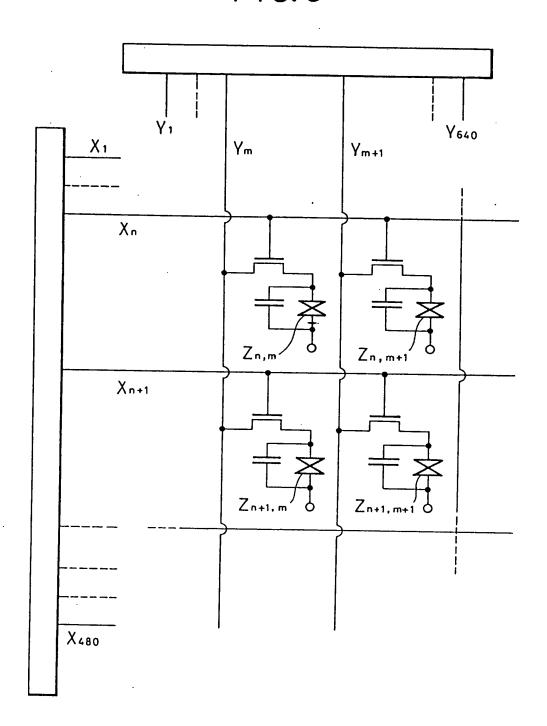
 $Z_{n,m}$: T1 + 2T1 = 3T1 - "3"

Zn+1,m : 4T1 - "4"

 $Z_{n,m+1}$: $4T_1 + 2T_1 = 6T_1 \rightarrow "6"$

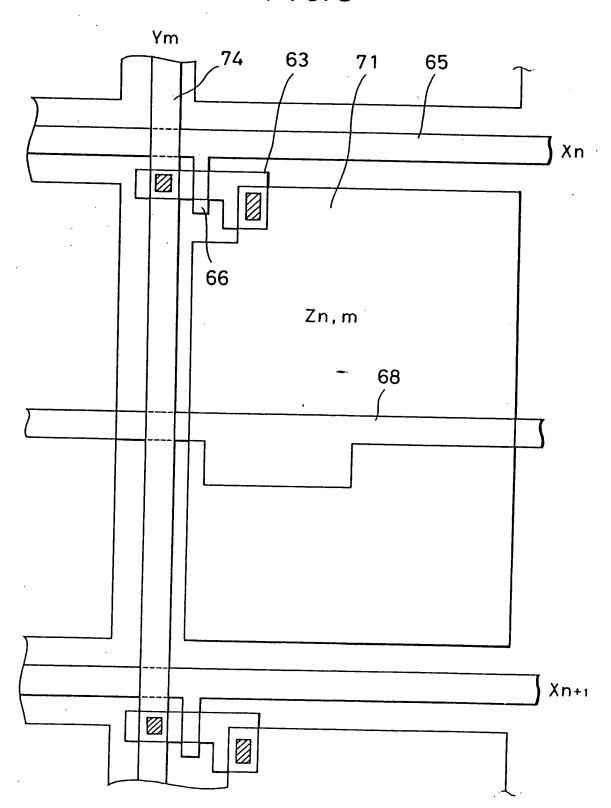
 $Z_{n+1,m+1}$: $T_1 + 4T_1 = 5T_1 - "5"$

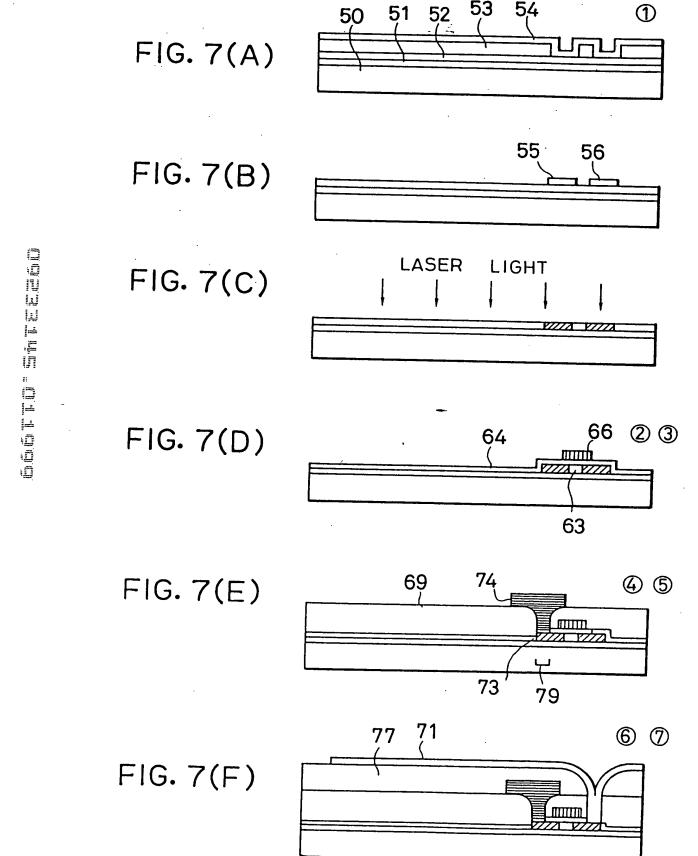
FIG.5



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FIG.6





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FIG. 8(A)

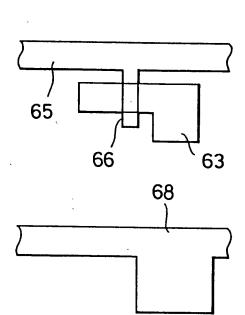


FIG. 8(B)

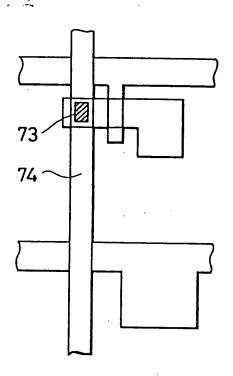


FIG.8(C)

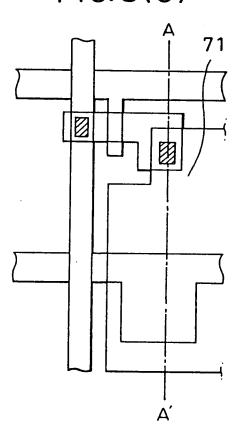
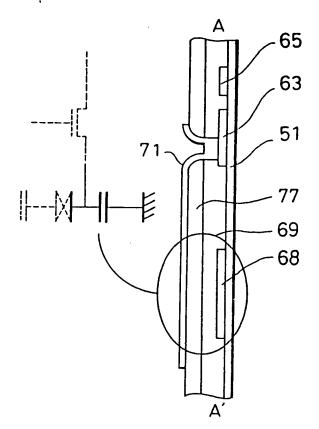
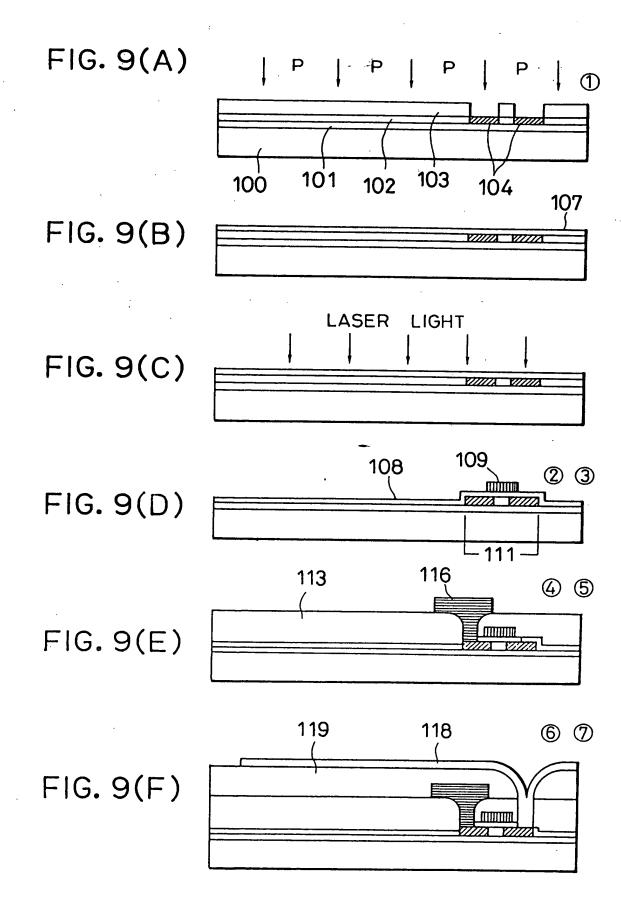


FIG.8(D)



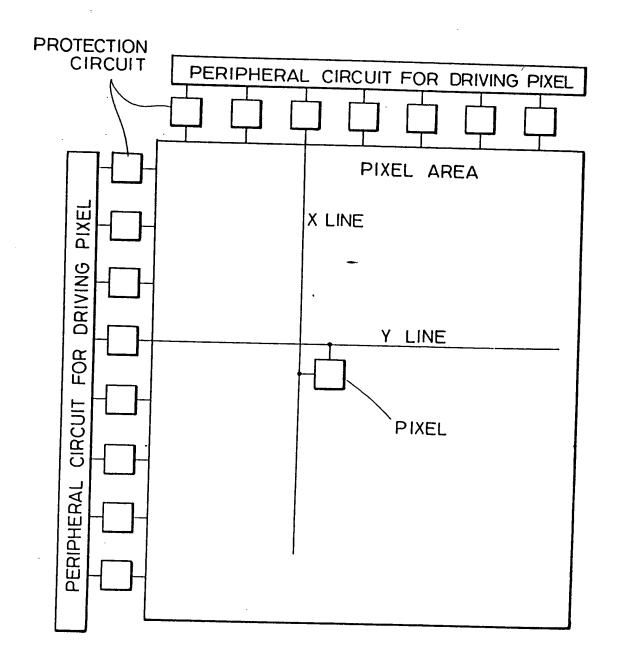


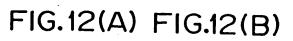


(1) (c) 6 $\begin{pmatrix} 1 \\ 2 \end{pmatrix}$ മ ပ 83 90 83 α α 86 ω 85 G α α FIG.10 (A) FIG. 10 (B) FIG. 10 (C) FIG. 10(D) FIG. 10(E)

Contraction of the contraction o

FIG. 11





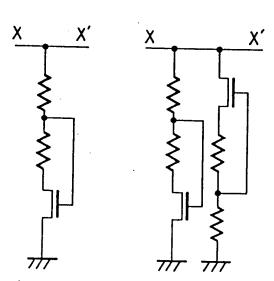


FIG.12(D)

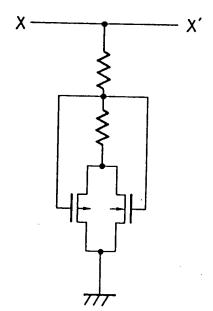


FIG.12(C)

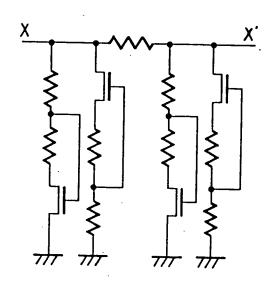
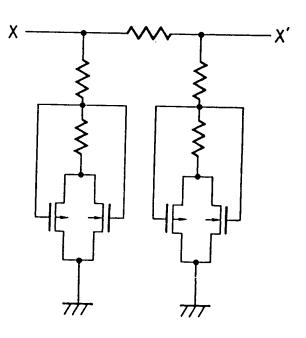
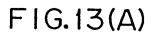


FIG.12(E)



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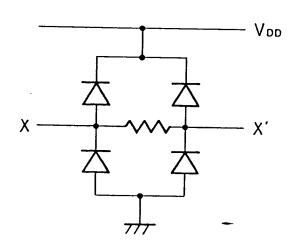


FIG.13(B)

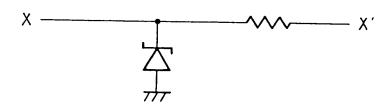
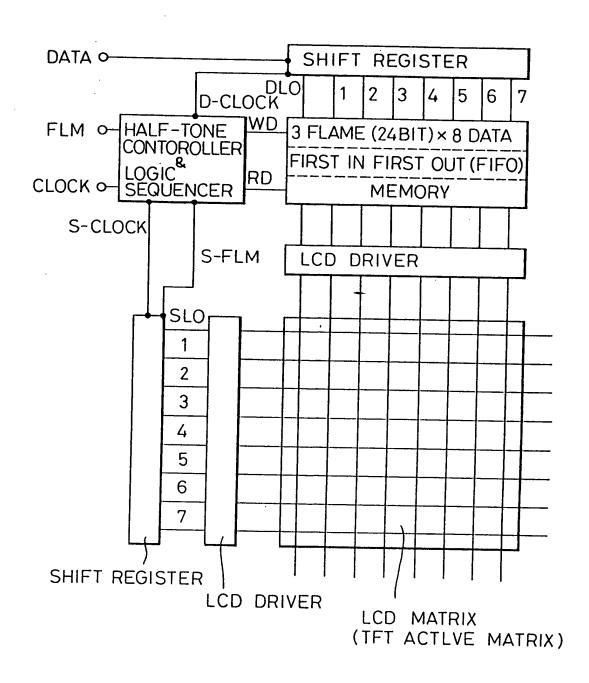


FIG.14.



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FIG. 15

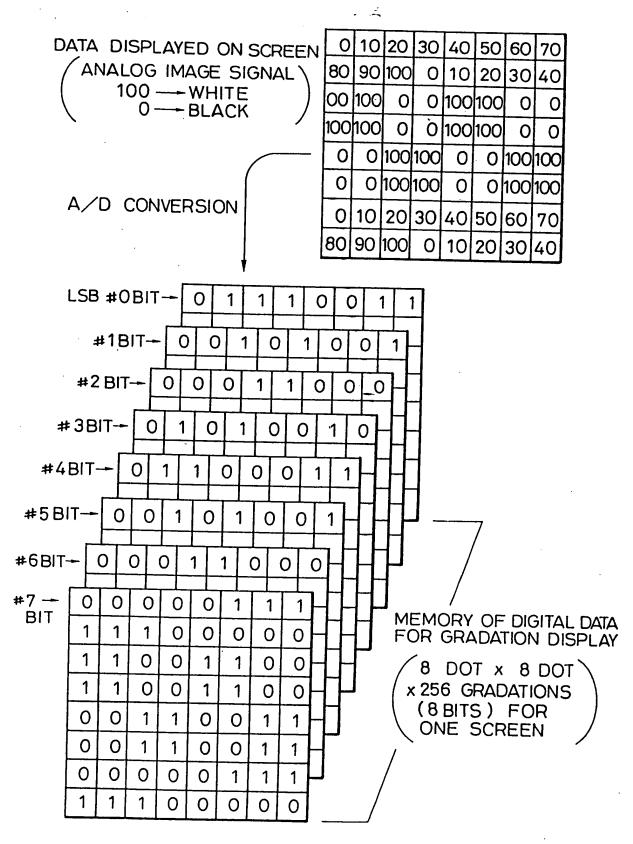
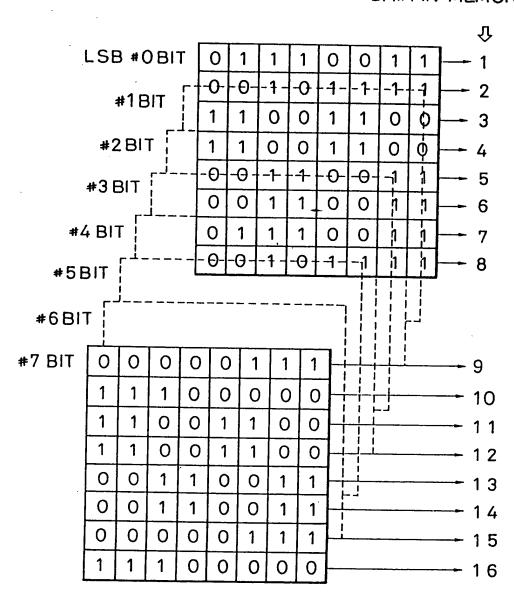


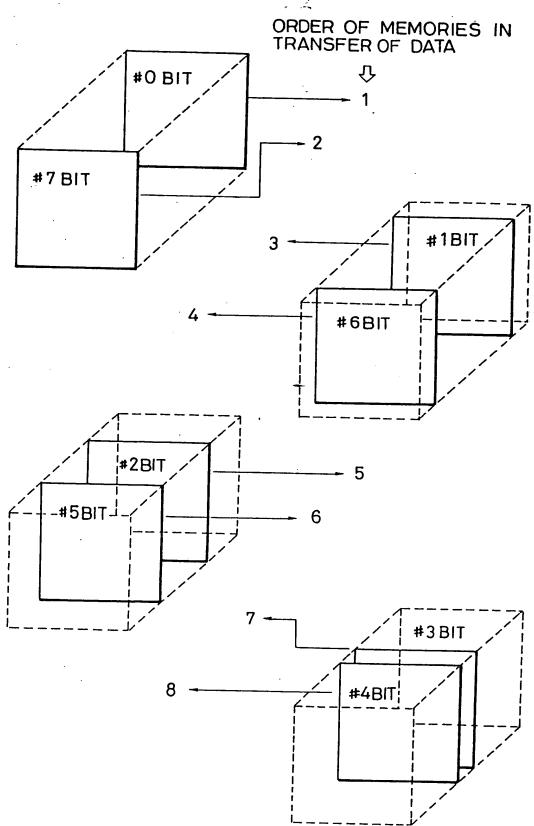
FIG. 16

ORDER OF TRANSFER OF DATA IN MEMORY



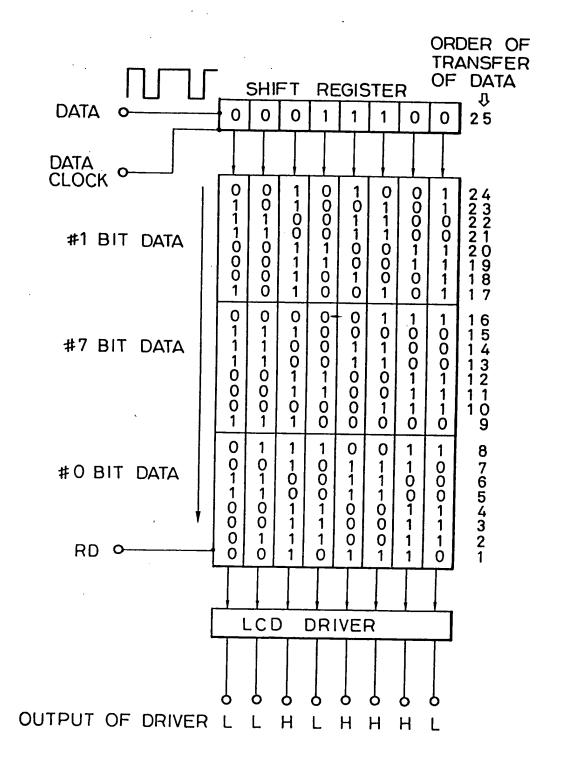
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FIG. 17



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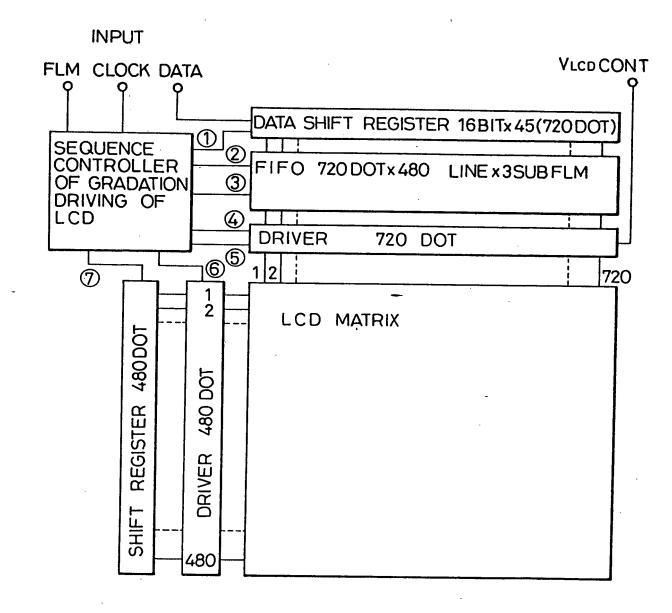
FIG. 18



16T #3BIT |#4BIT DISPLAY DISPLAY 817 24T 24 T 87 #7 BIT |#0 BIT |#7 BIT |#1 BIT |#6 BIT |#2 BIT |#5BIT | DISPLAY DISPLAY DISPLAY DISPLAY 32 T 36 T #0 BIT 24 T <u>1</u>7 #4 BIT **64T** 66 T #3 BIT **2**T #5BIT 128T 129T #2BIT -DATA TRANSFERRED #6BIT SL 0 9 FLM PL 9 **4001400** CLOCK FOR DATA TRANSFER FIG. 19

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FIG. 20



- ① DATA CLOCK
- 2 IN CLOCK
- 3 OUT CLOCK
- 4 DRIVE CLOCK
- ⑤ AC CLOCK
- **©** SET CLOCK
- THE SHIFT CLOCK

FIG. 21

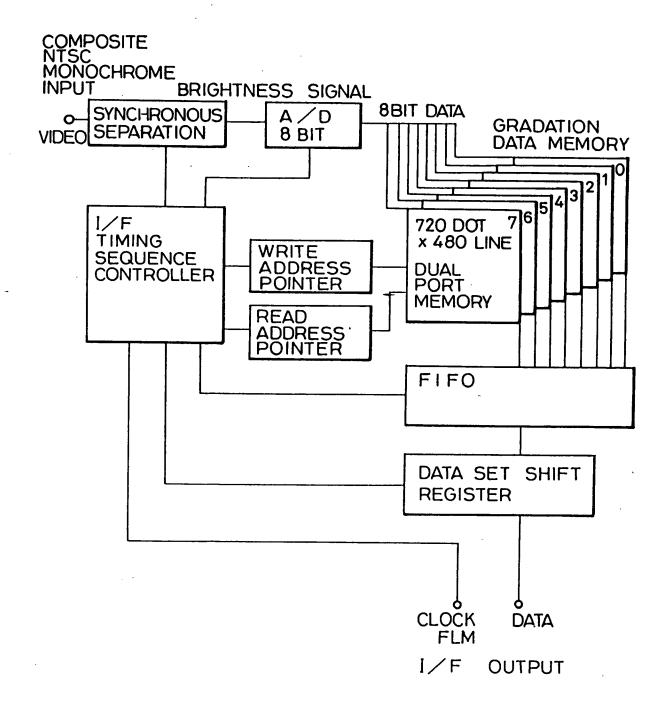


FIG. 22

<u>nazzzuk nilog</u>

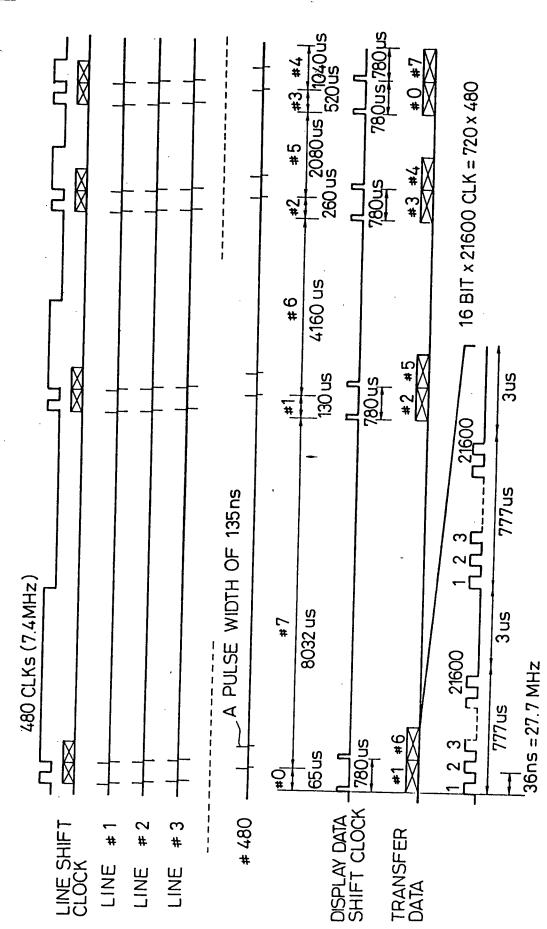
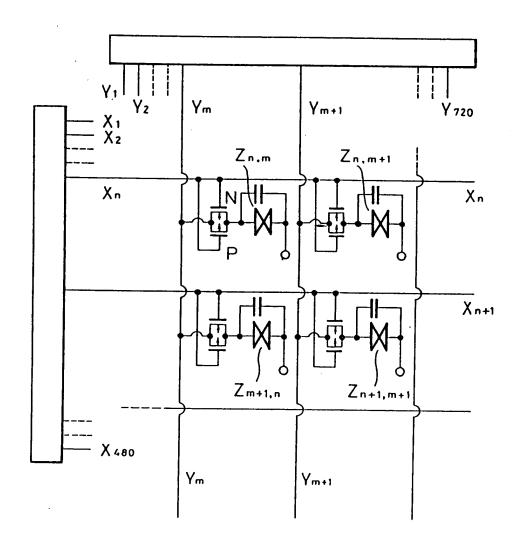


FIG. 23



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COBETAL DITGO



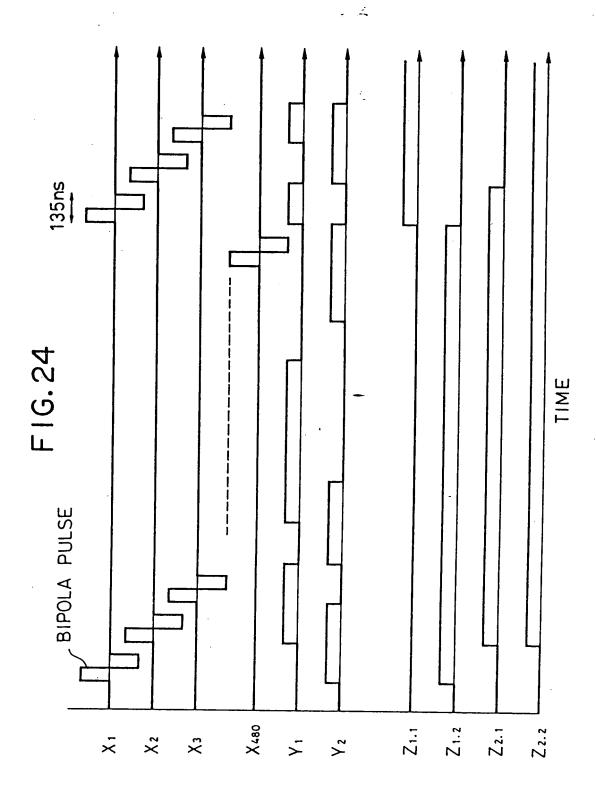


FIG. 25

